**REMARKS**

Claims 2, 5, 6, and 25 are pending in the above-identified application. Claim 2 has been amended herein.

Claims 2, 5, 6, and 25

Applicant respectfully requests reconsideration of the rejection of claims 2, 5, 6, and 25 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,333,206 ("Ito"), in view of U.S. Patent No. 5,878,943 ("Nishikawa"), in further view of U.S. Patent No. 6,330,967 ("Milewski"), in further view of U.S. Patent No. 5,633,533 ("Andros"). Claims 2, 5, 6, and 25 recite **solder bumps formed on the semiconductor chip**, the solder bumps forming spaces therebetween, **a resin film disposed on the semiconductor chip and the solder bumps**, the resin film being disposed in the spaces between solder bumps such that **upper surfaces of the solder bumps protrude from the resin layer**, a eutectic solder layer disposed on the cleaned upper surfaces of the solder bumps, a mounting board, a precoated solder layer disposed on the lands, wherein **the eutectic solder layer of the solder bumps *and* the precoated solder layer *join* the upper surfaces of the solder bumps to the lands** of the mounting board such that a stacked structure is obtained, wherein a gap is formed between the resin layer and the mounting board of the stacked structure.

Ito discloses a process for connecting a printed circuit board 1 to a semiconductor element 3 by flip-chip bonding. Nishikawa discloses a method for removing an oxide or contaminated layer from the surface of a solder material or bonding pad. Milewski discloses a process for connecting a circuit card 21 to an IC chip 10 via flip-chip bonding. Andros discloses a process for connecting a chip 41 to a layer 17 of a substrate 11 by wire bonding. Neither Ito, Nishikawa, Milewski, Andros, nor any combination of them shows or suggests solder bumps formed on the semiconductor chip, a resin film disposed on the semiconductor chip and the solder bumps, upper surfaces of the solder bumps protrude from the resin layer, the eutectic solder layer of the solder bumps *and* the precoated solder layer join the upper surfaces of the solder bumps to the lands, wherein a gap is formed between the resin layer and the mounting board.

The Office action relies on Milewski to show a pre-coated land. However, Milewski *teaches away* from the use of such precoated land ***and*** a coated solder ball, as the express purpose of Milewski is to obviate the need for both. The first teaching in Milewski of a coated land, referred to in the office action at page 3, lines 9-14, is with respect to the *prior art* of Milewski (col. 2, lines 56-57, and Fig. 3 caption) in which there is no eutectic coating on the solder ball (Fig. 3, and col. 2, lines 55-67). The primary embodiment of Milewski teaches a coated solder ball *in lieu of* a coated land (col. 4, line 47 to col. 5, line 5). Also, regarding that primary embodiment of Milewski, the solder ball coating 37 is not eutectic (col. 4, lines 53-56). In an alternate embodiment of Milewski having a coated land, the coated land is expressly used *instead of* a coated solder ball (col. 5, line 64-col. 6, line 1). Milewski purposely obviates the need for both a coated solder ball and a coated land, and thus teaches away from such use. Because Milewski teaches away from the use of a coated land with a coated solder ball, together, it is not reasonable to combine the Milewski teaching of a coated land with Ito's teaching of a coated solder ball (See MPEP 2141.02, stating, "(a) prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." (emphasis in original)).

The office action also asserts that Andros shows a gap between the resin layer 51 and the mounting board 27 and that it would have been obvious to combine Andros with the combination of Ito in view of Nishikawa and in further view of Milewski to teach the substance of present claim 25. However, the technology of Andros is quite different from and incompatible with the technologies of Ito, Nishikawa, Milewski, and the present invention. Andros discloses the connecting of a semiconductor chip 41 and a printed circuit board 27 via *wire bonding* (Fig. 4 and col. 5, lines 10-32). On the other hand, Ito, Nishikawa, Milewski, and the present invention teach *flip-chip* bonding, wherein solder bumps are used to connect a chip to a board. Instead of solder bumps formed on the chip, the wire bonding of Andros connects chip 41 to layer 17 of substrate 11 via wire 49 (col. 4, line 51-col. 5, line 32).

Because of their variant structures and uses, the resin in Andros cannot be logically combined with Ito to teach the claimed gap. Specifically, the resin 51 of Andros is not disposed *on* the solder bumps, as there are no solder bumps in wire bonding techniques. Rather, the resin of Andros is expressly implemented to

encapsulate the wires 49 (col. 5, lines 20-32). Flip-chip structure contains design limitations not present in wire bonding, and though a gap has been formed between a resin layer and a mounting board in a wire bonding technique (i.e., Andros), such a gap has hitherto not been formed in a flip-chip bonded structure with respect to resin disposed on the chip *and* the solder bumps as presently claimed.

Because Ito, Nishikawa, Milewski, and Andros fail, individually or in any logical combination, to show or suggest all of the elements of claims 2, 5, 6, and 25, the rejection of these claims is improper. Accordingly, Applicant respectfully requests that the rejection of these claims be withdrawn.

Conclusion

As it is believed that the application is in condition for allowance, a favorable action and Notice of Allowance are respectfully requested.

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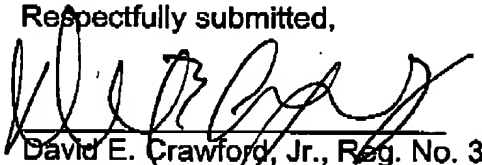
Respectfully submitted,



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